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Search Results -

Term	Documents
MULTI	840023
MULTIS	40
THREAD$4	0
THREAD	211031
THREADA	2
THREADABIY	3
THREADABLE	7272
THREADABLV	1
THREADABLY	63893
THREADABY	13
THREADAD	1
(L14 AND (THREAD$4 OR MULTI NEAR2 THREAD$3)).PGPB,USPT.	0

There are more results than shown above. Click here to view the entire set.

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Search: L15

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Results for "(((delay*, defer*, deter*, wait, postpon*) <near/15> branch* <near/15> (clock*, cycle..."

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(((delay*, defer*, deter*, wait, postpon*) <near/15> branch* <near/15> (clock*, cycle Search

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IET JNL	IET Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IET CNF	IET Conference Proceeding
IEEE STD	IEEE Standard

view selected items Select All Deselect All

1. **Compaction with general synchronous timing**
Allan, V.H.; Mueller, R.A.;
Software Engineering, IEEE Transactions on
Volume 14, Issue 5, May 1988 Page(s):595 - 599
Digital Object Identifier 10.1109/32.6137
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2. **Incorporating interconnect, register, and clock distribution delays into the retiming process**
Soyata, T.; Friedman, E.G.; Mulligan, J.H., Jr.;
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Volume 16, Issue 1, Jan. 1997 Page(s):105 - 120
Digital Object Identifier 10.1109/43.559335
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3. **A 2.5-GFLOPS, 6.5 million polygons per second, four-way VLIW geometry processor with Sl a software bypass mechanism**
Kubosawa, H.; Higaki, N.; Ando, S.; Takahashi, H.; Asada, Y.; Anbutsu, H.; Sato, T.; Sakate, M.; S Miyake, H.; Okano, H.; Asato, A.; Kimura, Y.; Nakayama, H.; Kimoto, M.; Hirochi, K.; Saito, H.; Kai Shimada, T.;
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Vallancourt, D.; Tsividis, Y.P.;
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5. **Design methodology for synthesizing clock distribution networks exploiting nonzero localiz**
Neves, J.L.; Friedman, E.G.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
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DB=PGPB,USPT; PLUR=YES; OP=OR

L15	L14 and (thread$4 or multi near2 thread$3)	0	L15
L14	L13 and unconditional	1	L14
L13	L12 and (compil$5 or assembl$5)	1	L13
L12	L7 and pipelin$6	1	L12
L11	L9 and l4	5	L11
L10	L9 and l1	8	L10
L9	(713/401,601)[CCLS]	976	L9

DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L8	(COUNT$3 OR NUMBER) NEAR5 (instruction$1 OR MICROINSTRUCTION$1) near15 (convert$5 or translat$6 or conversion$1 or calculat$4) near15 (delay$5 or wait$5)	53	L8
L7	5517628.pn.	2	L7
L6	L5 not l3	32	L6
L5	(detect$5 or determin$6 or check$4 count$5) near6 NUMBER NEAR5 (instruction$1) near15 (cycle$1 or clock$1) near15 (delay$5 or wait$5)	66	L5
L4	NUMBER NEAR5 (instruction$1) near15 (cycle$1 or clock$1) near15 (delay$5 or wait$5)	443	L4
L3	NUMBER NEAR5 (instruction$1) near15 (cycle$1 or clock$1) near15 (delay$5 or wait$5) near15 count$3	49	L3
L2	(instruction$1) near15 (cycle$1 or clock$1) near15 (delay$5 or wait$5) near12 number near15 count$3	80	L2
L1	(instruction$1) near15 (cycle$1 or clock$1) near15 (delay$5 or wait$5) near12 number	616	L1

END OF SEARCH HISTORY

Digital Object Identifier 10.1109/92.502201

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6. **On the complexity of designing optimal branch-and-combine clock networks**
El-Amawy, A.; Kulasinghe, P.;
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Digital Object Identifier 10.1109/12.664212

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7. **A novel image rejection architecture for quadrature radio receivers**
Valkama, M.; Renfors, M.;
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Volume 51, Issue 2, Feb 2004 Page(s):61 - 68
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8. **Retiming edge-triggered circuits under general delay models**
Lalgudi, K.N.; Papaefthymiou, M.C.;
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